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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,267	10/31/2003	Seiichi Watarai	088408/01DIV	9222

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,267	WATARAI, SEIICHI	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3 and 10-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3 and 10-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/101,936.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it is not narrative to the current invention application. Correction is required. See MPEP § 608.01(b).

2. The disclosure is objected to because of the following informalities: on the last line of page 12, numeral "12" should be changed to --21--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2, 3 and 10-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, "a data input means for the input of input data" on line 2 is indefinite because "the input" lacks antecedent basis, and it is not clear whether the above means that the data input means for providing the input data, or the data input means for receiving the input data. Appropriate correction and/or clarification is requested.

Also in claim 2, "a data latch means for latching the input data" on line 3 appears to be misdescriptive. Note that it is clearly so in Figure 2 that the data latch means (25, 26, 31, 32) connecting with the input data means (33, 34) for latching the outputs (Z, ZB) of the input circuit. Also note that it is also similar in other Figures as that the data latch means latching the outputs (Z, ZB) for similar reasons as discussed. Appropriate correction and/or clarification is requested.

Also in claim 2, "for blocking feedthrough current" on line 5 is indefinite because it is not known where the "feedthrough current" is coming from and/or which element(s) providing such current. Appropriate correction and/or clarification is requested.

Also in claim 2, "synchronizing the input of the input data to the data input means" is indefinite because it is so confusing and cannot be understood, and because of "the input of input data" is not clear as discussed above. Appropriate correction and/or clarification is requested.

In claim 3, "a data input means for the input of input data" on line 2 is indefinite for the same problem as discussed in claim 2 above.

Also in claim 3, "blocking feedthrough current" on line 3 is indefinite for the similar problem as discussed in claim 2 above.

Also in claim 3, "the reset state" on line 4 lacks antecedent basis and it is not clear the reset state of what (i.e., the reset state of the input circuit, the data latch means or other circuitry). Appropriate correction and/or clarification is requested.

Also in claim 3, "synchronizing the latch of the input data" on line 4 is indefinite because it is not clear how the data latch means synchronizing the latch of the input data. Further, it is seen in Figure 3 that the data latch means (37, 38 and 41-44) connected to the data input means (45, 46) for latching the outputs (Z, ZB) of the input circuit. Appropriate correction and/or clarification is requested.

Claims 10-12 are indefinite because they include the indefiniteness of claim 2.

Also in claim 10, "the second power source" on line 3 lacks antecedent basis.

Also in claim 11, "the first clock" on line 3 lacks antecedent basis.

Claims 13-14 are indefinite because they include the indefiniteness of claim 3.

Also in claim 13, "the nineteenth NMOS" on line 4 lacks antecedent basis; "the input end of the current path" on lines 4 and 7 lack antecedent basis and it is not clear whether they (both on lines 4 and 7) are the same with each other (i.e., are they the same "input end" and the same "current path"); "the eighteenth NMOS" on line 7 lacks antecedent basis; and "the output end of the current path" on lines 9-10 and 11-12 lack antecedent basis and it is not clear whether they (both on lines 9-10 and 11-12) are the same with each other (i.e., are they the same "output end" and the same "current path"). Appropriate correction and/or clarification is requested.

Also in claim 14, "a first input end" on line 3 is unclear antecedent basis since it is not known if it is the same as "the input end" recited on line 4 of claim 13; "a first output end" on line 4-5 is unclear antecedent basis since it is not known if it is the same as "the output end" recited on line 9-10 of claim 13; "a second input end" on line 6 is unclear antecedent basis since it is not known if it is the same as "the input end" recited on line 7 of claim 13; and "a second output end" on line 4-5 is unclear antecedent basis since it is not known if it is the same as "the output end" recited on line 8 of claim 13. Appropriate correction and/or clarification is requested.

With respect to claim 15, this claim is indefinite because it is not clear exactly which element(s) is/are for "a blocking feedthrough current unit" and which element(s) is/are for the "clock synchronization unit" beside other units recited in the input circuit. Note that reading in Figure 2, data input unit (33, 34), data latch (25, 26, 29, 30), reset unit (27, 28), clock synchronization unit (31, 32), latch enhancement unit (35 36); and there is no other element left for the "blocking feedthrough current unit". Note that, in Figure 2, if we read elements (31, 32) for the "feedthrough current unit", then there is no elements for the "clock synchronization unit".

Similarly, reading in Figure 3, data input unit (45, 46), data latch (37, 38, 41-44), reset unit (39, 40), latch enhancement unit (47, 48); and there is no other element left for the "blocking feedthrough current unit" and the clock synchronization unit. Appropriate correction and/or clarification is requested.

Also in claim 15, "a data input unit for inputting data" on line 2 is not clear for the similar reason as discussed in claim 2, i.e., it is not clear whether it is for receiving or for providing the input data. Appropriate correction and/or clarification is requested.

Also in claim 15, the recitation "a data latch for latching the input data" on line 3 is indefinite for the similar reason as discussed in claims 2 and 3 above. Further, "the input data" is unclear antecedent basis since it is not clear whether it is the same as "data" on line 2. Appropriate correction and/or clarification is requested.

Also in claim 15, "for synchronizing the input of the input data to the input data" on line 5 is indefinite because it is so confusing and cannot be understood, and because of "the input of input data" is not clear since it is not clear in the claim whether the data input unit for receiving or for providing the input data. Appropriate correction and/or clarification is requested.

Also, "a feedthrough current" on line 8 is indefinite for the similar reason as discussed in claim 2 above.

Claims 16 and 17 are indefinite because they include the indefiniteness of claim 15.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 2, 3, 10, 12, 15 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant Admitted Prior Art (AAPR), Figure 6.

Insofar as understood in claims 2, 3, 10, 12, 15 and 17, Figure 6 of the AAPR discloses a circuit, which includes: a data input means (7, 8), a data latch means (1, 2, 5, 6), a reset means (3, 4), a clock synchronization means (9) and a latch enhancement means (10, 11). Note that, for claim 2, the clock synchronization means (9) meets the limitation "for block feedthrough current" because when transistor 9 is OFF then no current can flow through, and also meets the limitation "synchronizing" because when transistor 9 is ON then the data input means operates. Also note that, for claim 3, the data latch means meets the meets the limitation "for block feedthrough current in the reset state" because in the reset state, transistor 9 is OFF so no current can flow through, and also meets the limitation "synchronizing the latch" because transistor 9 is ON and transistors 3-4 are OFF so the data input means operates and the causing the data latch means to latch.

7. Claims 2, 3, 10-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (USP 6,486,719).

Insofar as understood in claims 2, 10, 12, 15 and 17, Figure 8 of the Kim reference discloses a circuit, which includes: a data input means (NA, NC), a data latch means (N1, N3, P1, P2), a reset means (P0, P3), a clock synchronization means (NB, ND) and a latch

enhancement means (N0, N2). Note that, in Figure 8, the clock synchronization means (NB, ND) meets the limitation "for block feedthrough current" because when transistors NB and ND are OFF then no current can flow through, and also meets the limitation "synchronizing" because when transistors NB and ND are ON then the data input means operates. , Also note that claims 15 and 17 are met as it appears that the blocking feedthrough current unit is the same as the clock synchronization unit as discussed in the indefinite problem above.

Insofar as understood in claims 2, 10, 11, 12, 15 and 17, Figures 8 and 10 of the Kim reference discloses a circuit, which includes: a data input means (NA, NC), a data latch means (N1, N3, P1, P2), a reset means (P0, P3), a clock synchronization means (N0, N2) and a latch enhancement means (NB, ND). Note that claims 15 and 17 are met as it appears that the blocking feedthrough current unit is the same as the clock synchronization unit as discussed in the indefinite problem above.

Insofar as understood in claims 3, 15 and 16, Figure 10 of the Kim reference discloses a circuit, which includes: a data input means (NA, NC), a data latch means (N1, N3, P1, P2, N0, N2), a reset means (P0, P3), and a latch enhancement means (NB, ND). Note that the data latch means meets the meets the limitation "for block feedthrough current in the reset state" because in the reset state, transistors N0 and N2 are OFF so no current can flow through, and also meets the limitation "synchronizing the latch" because transistors N0 and N2 are ON and transistors P0 and P3 are OFF so the data input means operates and the causing the data latch means to latch; and claims 15 and 16 are met as it appears that the data latch provides blocking feedthrough current function and synchronizing function as discussed in the indefinite problem above.

Insofar as understood in claims 3 and 13-16, Figure 6 of the Kim reference discloses a circuit, which includes: a data input means (NB, ND), a data latch means (NA, NC, N0, N2, P1, P2), a reset means (P0, P3), and a latch enhancement means (N1, N3). Note that the data latch means meets the meets the limitation "for block feedthrough current in the reset state" because in the reset state, transistors N0 and N2 are OFF so no current can flow through, and also meets the limitation "synchronizing the latch" because transistors N0 and N2 are ON and transistors P0 and P3 are OFF so the data input means operates and the causing the data latch means to latch; and claims 15 and 16 are met as it appears that the data latch provides blocking feedthrough current function and synchronizing function as discussed in the indefinite problem above. Also note in Figure 6 is that the first PMOS (P1), the second PMOS (P2), the nineteenth NMOS (NC), the sixteenth NMOS (N0), the seventeenth NMOS (N2).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 10, 2004

Long Nguyen
Primary Examiner
Art Unit: 2816